CLAIMS

1. A method for testing an integrated circuit, the method comprising:

receiving a first failing region, the first failing region corresponding to one or more circuits on the integrated circuit;

generating a set of adaptive algorithmic test patterns for the one or more circuits in response to the first failing region and to a logic model of the integrated circuit;

determining expected results for the test patterns;

applying the test patterns to the first failing region on the integrated circuit resulting in actual results for the test patterns;

comparing the expected results to the actual results;

transmitting mismatches between the expected results and the actual results to a fault simulator; and

receiving a second failing region from the fault simulator, the second failing region created in response to the mismatches and the logic model, and the second failing region corresponding to a subset of the first failing region.

2. The method of claim 1 wherein the first failing region is identified from the fault simulator.

3. The method of claim 1 wherein the generating, determining, applying, comparing, transmitting and receiving a second failing region are repeated with the value of the second failing region being substituted for the first failing region, until the second failing region corresponds to a failing gate.

4. The method of claim 1 wherein the generating, determining, applying, comparing, transmitting and receiving a second failing region are repeated with the value of the second failing region being substituted for the first failing region, a selected number of times.

5. The method of claim 1 further comprising receiving one or more diagnostic classes corresponding to the second failing region from the fault simulator, wherein the generating, determining, applying, comparing, transmitting, receiving a second failing region and receiving one or more diagnostic classes are repeated with the value of the second failing region being substituted for the first failing region, until less than a selected number of diagnostic classes are received for the second failing region.

6. The method of claim 1 further comprising receiving one or more conditions corresponding to the first failing region from the fault simulator, wherein the generating, determining, applying, comparing, transmitting and receiving a second failing region are repeated with the value of the conditions being varied.

7. The method of claim 6 wherein the conditions include one or more of voltage, cycle and temperature.

8. The method of claim 1 wherein determining expected results is performed by executing an operating region corresponding to the failing region in the integrated circuit that was identified during initial testing.

9. The method of claim 1 wherein determining expected results is performed by executing an operating region corresponding to the failing region in another integrated circuit.

10. The method of claim 1 wherein determining expected results is performed by executing a simulation corresponding to the failing region.

11. The method of claim 1 wherein the set of algorithmic test patterns include one or more of walk, march, checkerboard and exhaustive.

12. The method of claim 1 wherein the set of algorithmic test patterns are characterized as one or more of deterministic, pseudo-random and functional.

13. A computer program product for testing an integrated circuit, the computer program product comprising:

a storage medium readable by a processing circuit and storing instructions for execution by the processing circuit for performing a method comprising:

receiving a first failing region, the first failing region corresponding to one or more circuits on the integrated circuit;

generating a set of adaptive algorithmic test patterns for the one or more circuits in response to the first failing region and to a logic model of the integrated circuit;

determining expected results for the test patterns;

applying the test patterns to the first failing region on the integrated circuit resulting in actual results for the test patterns;

comparing the expected results to the actual results;

transmitting mismatches between the expected results and the actual results to a fault simulator; and

receiving a second failing region from the fault simulator, the second failing region created in response to the mismatches and the logic model, and the second failing region corresponding to a subset of the one or more circuits on the integrated circuit.

14. The storage medium of claim 13 wherein the generating, determining, applying, comparing, transmitting and receiving a second failing region are repeated with the value of the second failing region being substituted for the first failing region, until the second failing region corresponds to a failing gate.

15. The storage medium of claim 13 wherein the generating, determining, applying, comparing, transmitting and receiving a second failing region are repeated with the value of the second failing region being substituted for the first failing region, a selected number of times.

16. The storage medium of claim 13 further comprising receiving one or more diagnostic classes corresponding to the second failing region from the fault simulator, wherein the generating, determining, applying, comparing, transmitting, receiving a second failing region and receiving one or more diagnostic classes are repeated with the value of the second failing region being substituted for the first failing region, until less than a selected number of diagnostic classes are received for the second failing region.

17. The storage medium of claim 13 further comprising receiving one or more conditions corresponding to the first failing region from the fault simulator, wherein the generating, determining, applying, comparing, transmitting and receiving a second failing region are repeated with the value of the conditions being varied.

18. A system for testing an integrated circuit, the system comprising:

a programmable pattern generator;

a bootstrapping module in communication with the integrated circuit; and

a test controller in communication with the programmable pattern generator, the bootstrapping module, the integrated circuit and a fault simulator including a logic model of the integrated circuit, the test controller including instructions to execute the method comprising:

receiving a first failing region, the first failing region corresponding to one or more circuits on the integrated circuit;

generating a set of adaptive algorithmic test patterns for the one or more circuits in response to the first failing region and to the logic model, wherein the algorithmic test patterns are created by the programmable pattern generator;

determining expected results for the test patterns, wherein the expected results are captured by the bootstrapping module;

applying the test patterns to the first failing region on the integrated circuit resulting in actual results for the test patterns, wherein the actual results are captured by the bootstrapping module;

comparing the expected results to the actual results;

transmitting mismatches between the expected results and the actual results to the fault simulator; and

receiving a second failing region from the fault simulator, the second failing region created in response to the mismatches and the logic model, and the second failing region corresponding to a subset of the one or more circuits on the integrated circuit.

19. The system of claim 18 wherein the integrated circuit is a level sensitive scan design device.

20. The system of claim 18 wherein the integrated circuit is a very large-scale integration device.